YRM-8P-101

869MHz Radio Modem, 500mW (+27dBm) Transmit Power,
5ppm timing and frequency accuracy

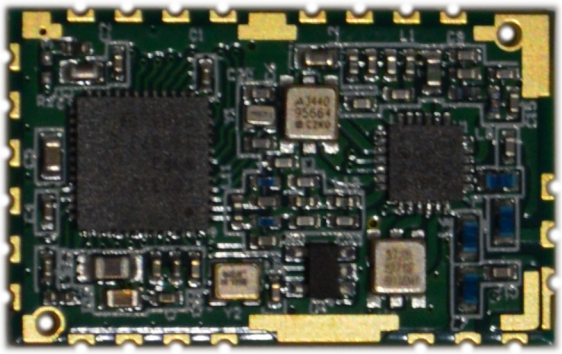
Features

RF

- EU860 free license band
- 500mW (+27dBm) output power
- Embeds SAW filter and LNA for high reception sensitivity
- High efficiency Tx Power amplifier
- 2 Selectable Antenna outputs
- 5 ppm TCXOs for timing and frequency accuracy and stability
- Low current consumption
    - <12mA in receive mode
    - <500mA @ 3.3V, 500mW (+27dBm) output power
    - <2uA in sleep mode
- Outdoor range line-of-sight: up to 30km w/ dipole antenna
- Suitable for Systems Targeting Compliance With Europe ETSI: EN 300220 Cat 1.5, EN 303131, EN 303204

Protocol and Networking

- Available software stacks
    - TDMA (Time Division Multiple Access)
    - FHSS (Frequency Hoping)
    - IEEE 802.15.4g, Wi-SUN® FAN1.0
    - Mesh networking
- API commands to control packet routing
- 2-GFSK, 4-GFSK, MSK modulations
- FEC (Forward Error Correction)
- Digital RSSI information
- UART interface with flow control
- Hardware protocol status tracking



Special Features

- 2.0V - 3.3V power supply (for battery operation)
- Industrial grade temperature range from -40° to 85°C
- 4 general purpose IO
- Serial wire JTAG debug port
- Small form factor (29.5mm x 18mm)

Typical Applications

- Wi-SUN® Field and Home Area Networks
- Narrowband Ultra-Low-Power Wireless Systems
- Wireless Metering (AMR) and Smart Grid (AMI)
- Wireless Sensor Networks
- Wireless Healthcare Applications
- Industrial Monitoring and Control
- Home and Building Automation

1. Overview

The YRM-8P-101 is a high performance, long range, drop-in radio module for seamless integration.

With its small form factor, this Radio Module (RM) can easily replace miles of cables in industrial applications. The radio module is built to ensure highly reliable data communications in multi-node networks and harsh environments.

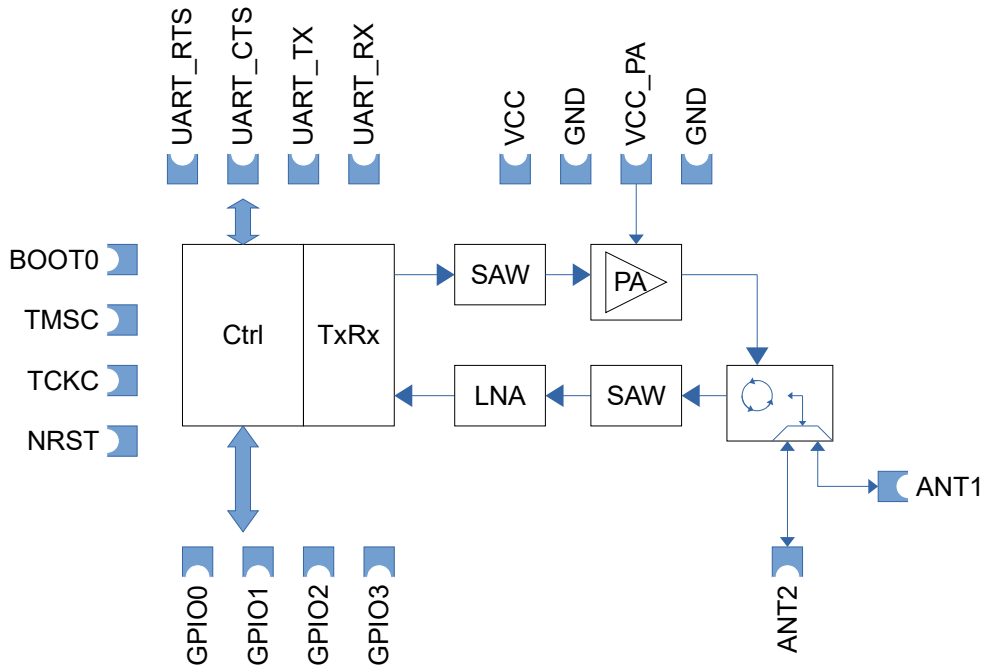


Figure 1: Block Diagram

The Radio Module includes a communication controller with embedded radio communication software, an RF transceiver (TxRx), a power amplifier (PA) to deliver up to 500mW (+27dBm), SAW filters placed both on the Tx and the Rx paths and an antenna switch for selecting between two antennas.

The communication controller handles the radio packet protocol, the communication interfaces, the generic I/O signals and controls the RF transceiver. Data is exchanged with the host using a generic UART interface.

This module works with the embedded firmware:

- YFW-TD-002, dedicated to TDMA applications;
- YFW-TD-003, dedicated to FHSS applications;

1.1. Pinout description

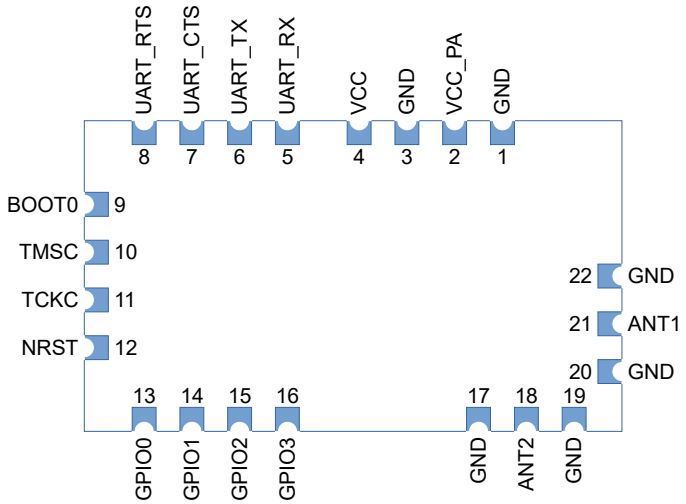


Figure 2: Pinout

Pin#	Type	Name	Function
1	P	GND	Ground
2	P	VCC_PA	Power Amplifier supply
3	P	GND	Ground
4	P	VCC	Power supply
5	I	UART_RX	UART reception line
6	O	UART_TX	UART transmission line
7	I	UART_CTS	UART clear to send
8	O	UART_RTS	UART ready to receive
9	I	BOOT0	Active high reprogramming selection
10	I	TMSC	cJTAG MS (do not connect-for internal use only)
11	I	TCKC	cJTAG clock (do not connect-for internal use only)
12	I	NRST	Active low system reset
13	I(O)	GPIO0	General Purpose I/O
14	I(O)	GPIO1	General Purpose I/O
15	I(O)	GPIO2	General Purpose I/O
16	I(O)	GPIO3	General Purpose I/O
17	P	GND	Antenna #2 ground plane
18	A	ANT2	Antenna #2
19	P	GND	Antenna #2 ground plane
20	P	GND	Antenna #1 ground plane
21	A	ANT1	Antenna #1
22	P	GND	Antenna #1 ground plane

P=Power; I=Digital Input; O=Digital Output; A=Analog

1.2. Specifications

Conditions : V_{CC}=3.3V, T_A=25°C if not specified otherwise

DC characteristic	Min	Typ	Max	Unit	Comments
Power supply VCC	2.0		3.3	V	
PA supply VCC_PA	2.0		4.8	V	
Transmitter current					
			500	mA	Power output 500mW
Receiver current			12	mA	
Sleep Mode			2	uA	

Conditions : V_{CC}=3.3V, TX power +27dBm, T_A=25°C if not specified otherwise

RF performance	Min	Typ	Max	Unit	Comments
TX output power	2		500	mW	Software selectable
	3		27	dBm	
Data rate			1000	kbps	
RX sensitivity		-112		dBm	BW=100kHz GFSK-2 @ BER=10^{-3}
Phase Noise		-101		dBc/Hz	±10kHz offset
Antenna output impedance		50		ohm	Unbalanced
Frequency	860		870	MHz	

I/O (GPIO, UART)	Min	Typ	Max	Unit	Comments
Digital inputs VIH	0.8xVCC			V	
Digital inputs VIL			0.2xVCC	V	
Digital outputs VOH	VCC-0.4			V	
Digital outputs VOL			0.4	V	

NRST pin characteristics	Min	Typ	Max	Unit	Comments
VIH input high level	0.8xVCC			V	
VIL input low level			0.2xVCC	V	
Rpu weak pull-up		100		kohm	
Low duration	1			us	

Not tested

Absolute MAX	Min		Max	Unit	Comments
Supply Voltage VCC Pin	-0.3		3.6	V	
Supply Voltage VCC_PA Pin	-0.3		4.8	V	
Voltage on any dig pin(1)	-0.3		3.6	V	VDD+0.3 or max 4.1V

2. HARDWARE DESCRIPTION

The radio module hardware implements an ultra low power system-on-chip with integrated *Arm® Cortex®-M4F 32-bit CPU with embedded high-performance sub-GHz transceiver*, a *High-Power RF Front-End circuit*, other than AEC-Q200 qualified SAW filters.

All components have been carefully selected for their high-reliability, performance and integration.

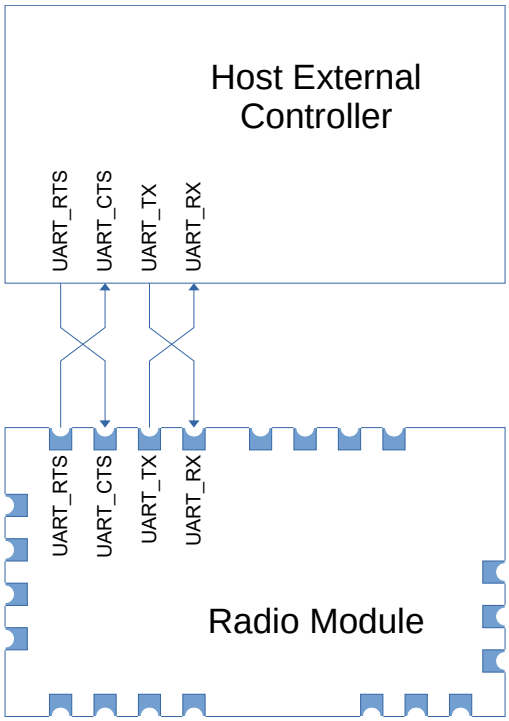
2.1. Antennas

Two selectable antennas are available. This feature may for example be useful in applications where an on board chip antenna and an off board dipole are necessary.

Note however that only one antenna can be enabled at a time (xor).

2.2. UART

The module interfaces to a host controller through one universal (a)synchronous receiver transmitter (UART) communication port.



The serial UART communication needs to be configured with the correct parameters (baud rate, parity, start and stop bits) for successful communication.

Default parameters are 9600 bps, no-parity, 1-stop, no-flow-control.

Each data packet consists of a start bit (low level), 8 data bits (LSB first) and one stop bit (high level). The following diagram illustrates the serial UART pattern to transfer data or commands to the radio module.

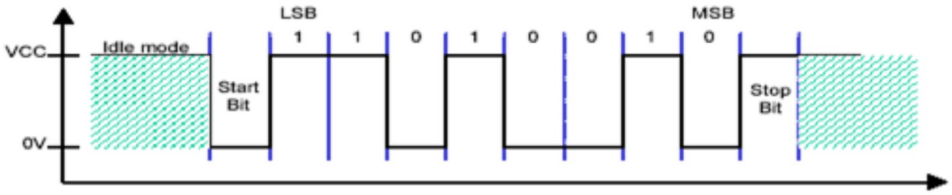


Figure 3: UART Data Packet (example 0x2B)

2.3. GPIO

GP[0..3] serve as general purpose pins. Reading or writing to these pins can be performed using the Utility Commands (details can be found in the Command Reference Manual).

2.4. NRST

The system reset pin NRST is connected to a first order RC circuit, that will ensure power-on reset. See specifications for component values.

2.5. JTAG

Pins TMSC and TCKC are used for cJTAG programming.

TMSC has an internal pull-up activated at power-up.

2.6. BOOT

This pin is used to select the reprogramming of the module. Three options are made available : from user Flash, from system memory, from embedded SRAM.

The boot loader is located in system memory. It is used to reprogram the Flash memory by using UART in Device mode through DFU (device firmware upgrade).

A Flash empty check mechanism is implemented to force the boot from system memory if the first flash memory location is not programmed and if the boot selection is configured to boot from main flash.

3. Typical Application

Figure below shows one typical application schematic using the radio module.

We recommend using two 47µF ceramic capacitors on both power supplies to help provide the peak current drawn by the module.

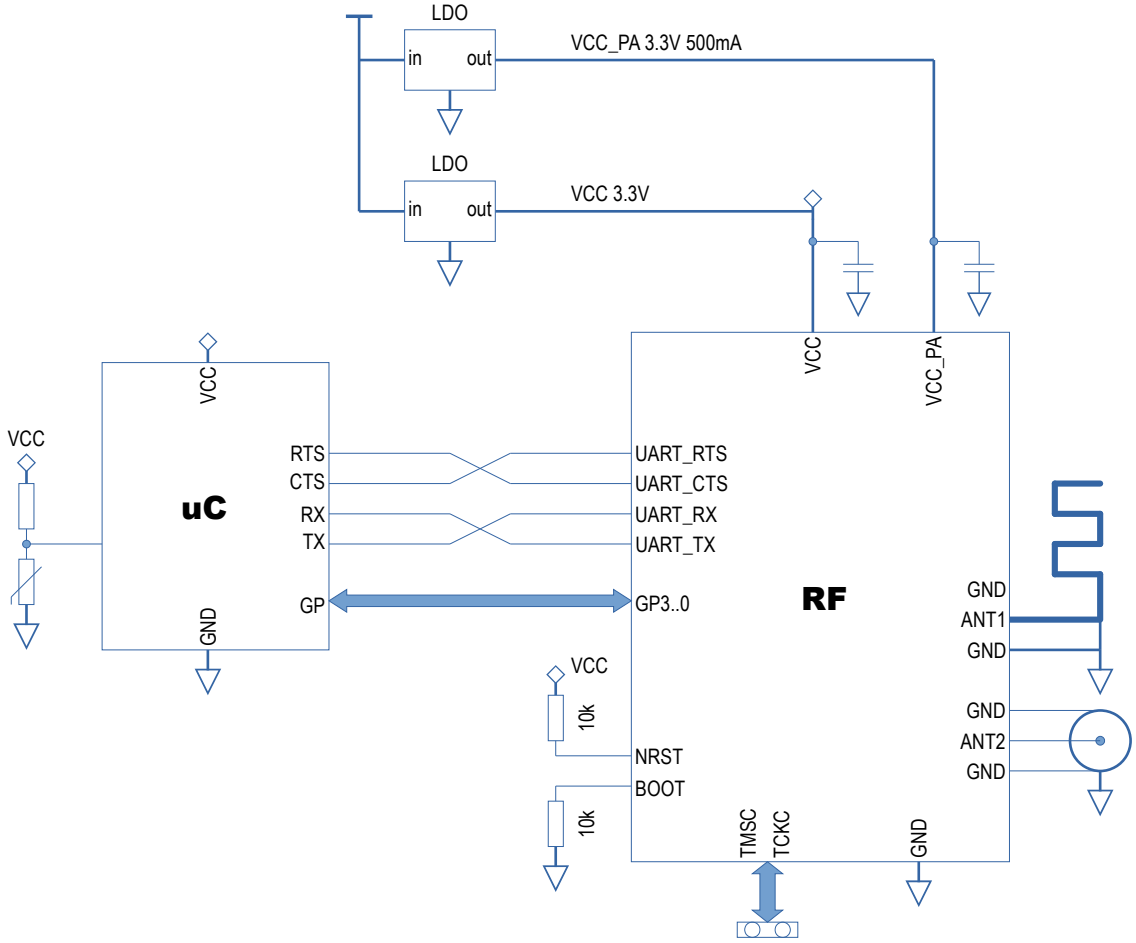


Figure 4: typical application

3.1. PCB layout guidelines

It is very important to pay attention to the RF section layout for optimum performance. A poor layout can cause lower output power, sensitivity degradation, etc.

We recommend the following general layout rules:

- Create a solid ground plane and ground vias under the module for system stability and thermal dissipation.
- Avoid signal routing underneath the module, especially on a layer where the module is mounted.

4. Mechanical information

QUAD FLAT MODULE

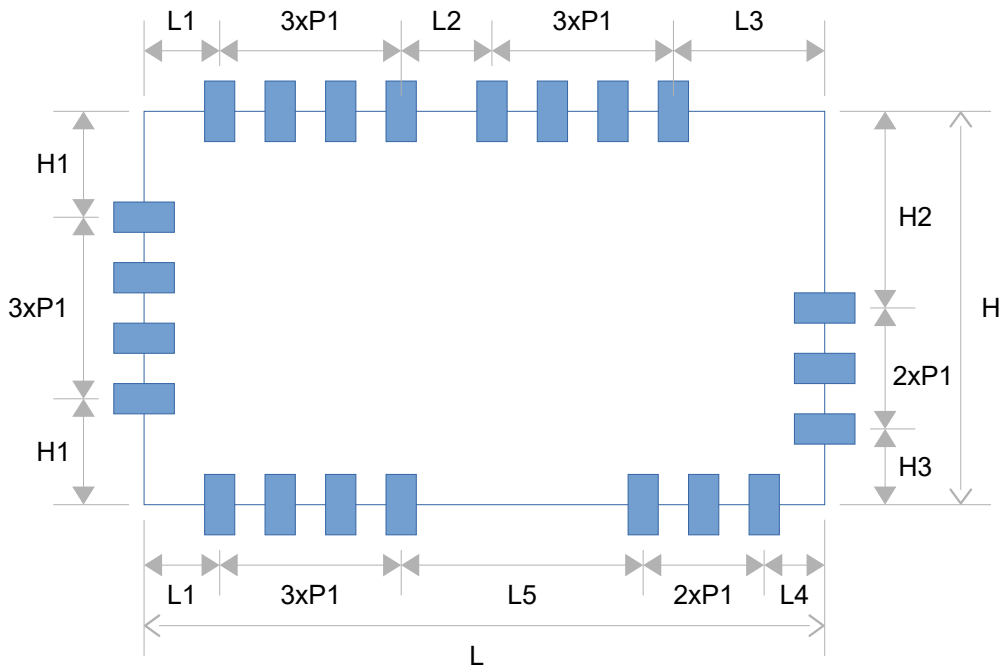


Figure 5: Footprint dimensions

		mm	mils
Length	L	29.5	1161.42
Height	H	18.0	708.66
Thickness (w/ shield)*	T	5.00	196.85
Pitch	P1	2.54	100
Horizontal lengths	L1	4.0	157.48
	L2	4.8	188.98
	L3	5.46	214.96
	L4	2.22	87.40
	L5	10.58	416.54
Vertical heights	H1	5.19	204.33
	H2	9.46	372.44
	H3	3.46	136.22

5. Revision History

0.3	Initial revision	February 2021

6. Contact

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